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Ghosh, D.; Nandy, S.K.;

VLSI Signal Processing, VI, 1993., [Workshop on] , 20-22 Oct. 1993

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2 A 100-MHz 2-D discrete cosine transform core processor

Uramoto, S.; Inoue, Y.; Takabatake, A.; Takeda, J.; Yamashita, H.; Terane, H.; Yoshimoto, M.;

Solid-State Circuits, IEEE Journal of , Volume: 27 , Issue: 4 , April 1992

Pages:492 - 499

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3 A programmable power-efficient decimation filter for software radios

Farag, E.N.; Ran-Hong Yan; Elmasry, M.I.;

Low Power Electronics and Design, 1997. Proceedings., 1997 International Symposium on , 18-20 Aug. 1997

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4 CORDIC versus conventional logic for realisation of normalised lattice all-pass filters

Nikolaidis, S.S.; Metafas, D.E.;

Electronics, Circuits, and Systems, 1996. ICECS '96., Proceedings of the Third IEEE International Conference on , Volume: 1 , 13-16 Oct. 1996

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5 The COREWARE methodology: building a 200 MFLOP processor in 9 man months

Stearns, C.; Harrington, T.; Stenbeck, A.;

ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE International , 21-25 Sept. 1992

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6 Power-efficient multiplier-accumulator design for FIR filters*Farag, E.N.; Ran-Hong Yan; Elmasry, M.I.;*

Electrical and Computer Engineering, 1997. IEEE 1997 Canadian Conference on , Volume: 1 , 25-28 May 1997

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